CHARACTERIZATION AND SIMULATION METHODOLOGY FOR TIME-DEPENDENT VARIABILITY IN ADVANCED TECHNOLOGIES

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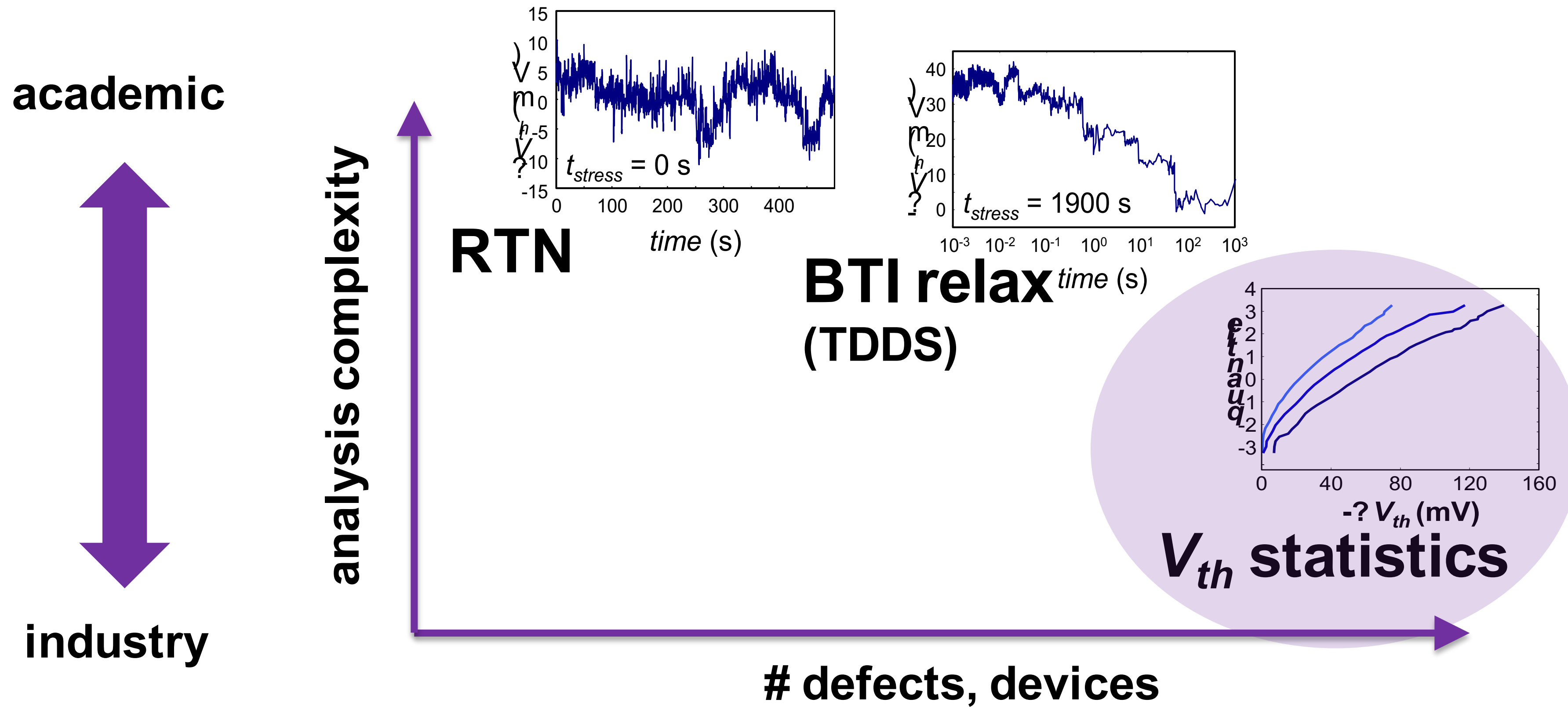
MOTIVATION: PARADIGM SHIFT IN ANALYZING TIME-DEPENDENT VARIABILITY IS NEEDED

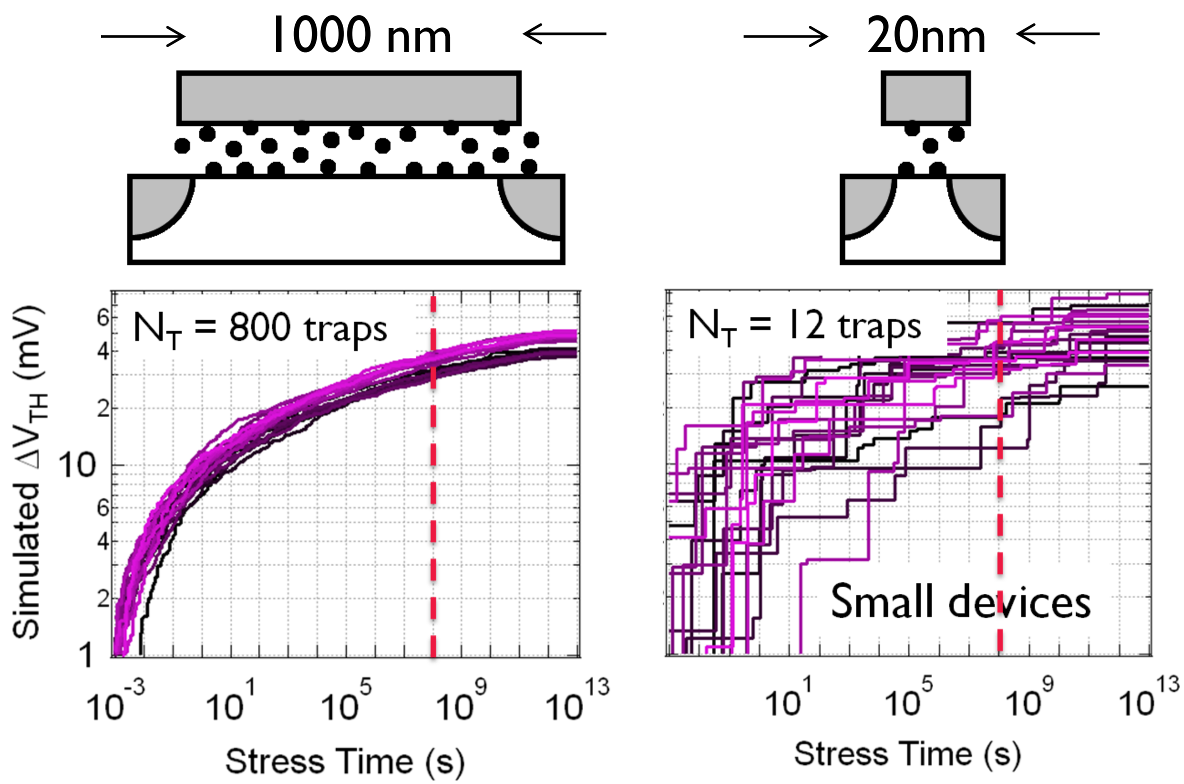


- Need for high-level abstraction tools (statistics) to deal with time-0 and time-dependent variability
- Need to maintain link to microscopic physics & technology

OUTLINE OF THIS TALK

- **Introduction to BTI and RTN variability**
- Test structure for characterization
  - Array design
  - Ideal DUT control
  - Measuring
- Modeling and analyzing
  - Defect centric BTI
  - Time and Voltage acceleration
  - Combined time-0 and time-dependent variability
- Importance of incorporating time-dependent

BIAS TEMPERATURE INSTABILITY



<u>Large devices</u>: random properties average out, resulting in a well defined lifetime

<u>Small devices:</u> the stochastic nature of the few defects results in increased spread

Tutorial by J. Franco, ICICDT, 2015

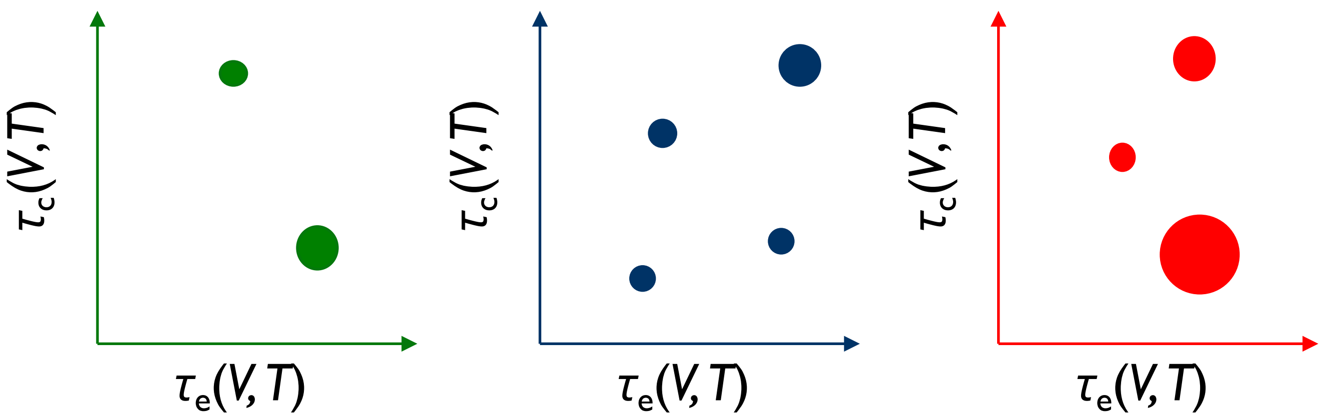
UNIFIED BTI & RTN STATISTICS CHARACTERIZED BY

- **capture time τ_c**
- **emission time τ_e**
- **impact on device** (ΔI_d or ΔV_{th},...)
- occupancy (0 or 1) at given time

Depend on
- spatial position
- energy position
- lattice relax. energy
- ...

Each device is characterized by:
- **number of defects N_T (~Pois(<N_T>))** with above properties

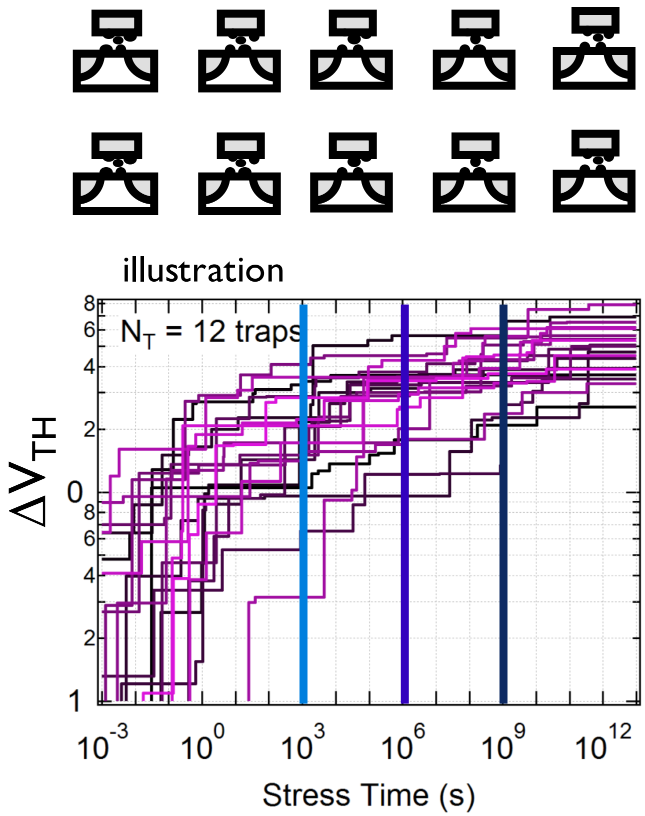
Example: defects in 3 different devices

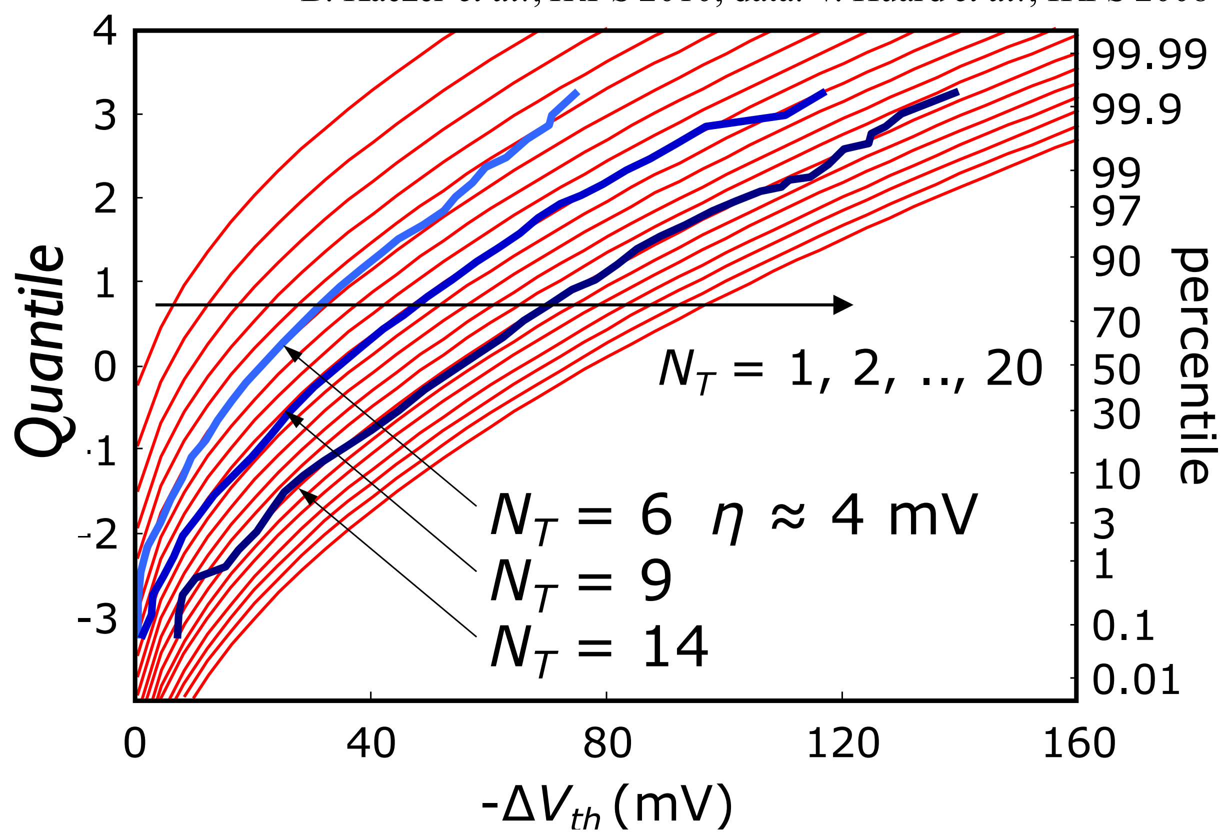


(size of bubble represents impact)

BTI STATISTICS FULLY DESCRIBED BY IMPACT PER DEFECT η AND NUMBER OF ACTIVE DEFECTS N_T

B. Kaczer *et al.*, *IRPS* 2010; data: V. Huard *et al.*, IRPS 2008





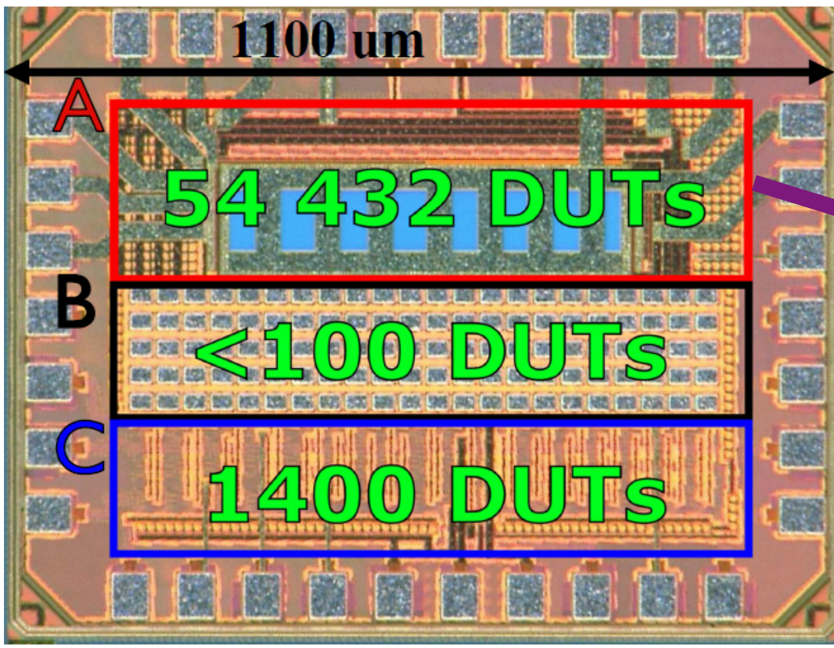
$$H_{\eta,N_T}(\Delta V_{th}) = \sum_{n=0}^{\infty} \frac{e^{-N_T} N_T^n}{n!} \left[1 - \frac{n}{n!} \Gamma(n, \Delta V_{th}/\eta) \right]$$

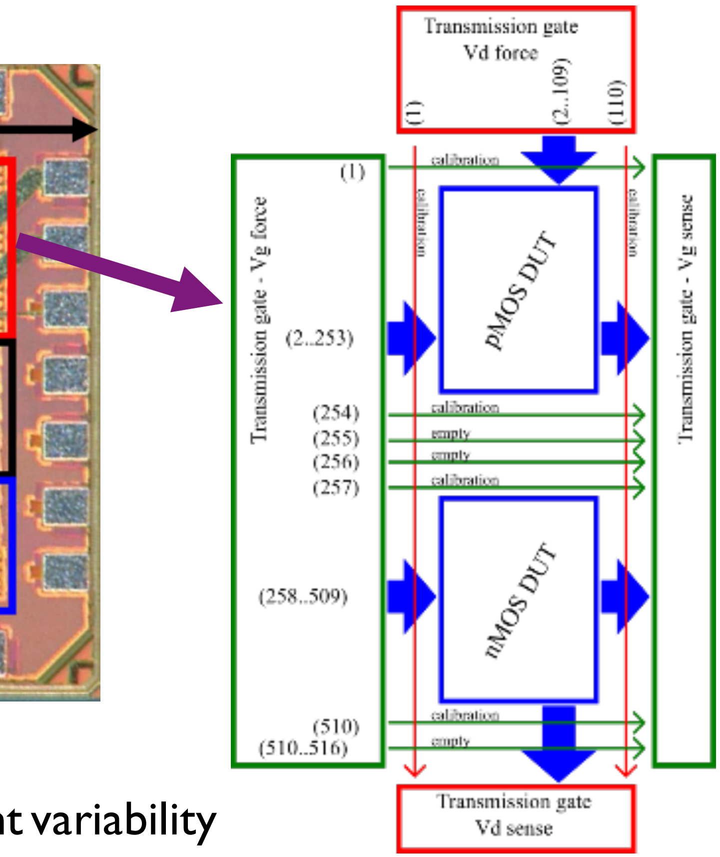
η = ⟨single defect impact⟩

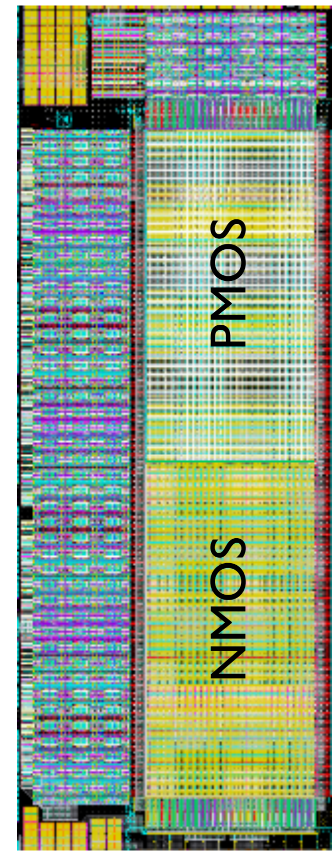
$N_T(t)$ = ⟨# of active defects per device⟩

Known statistics→ all moments can be derived

VARIABILITY TEST ELEMENT GROUP (TEG) NEEDED FOR RELIABILITY EVALUATION



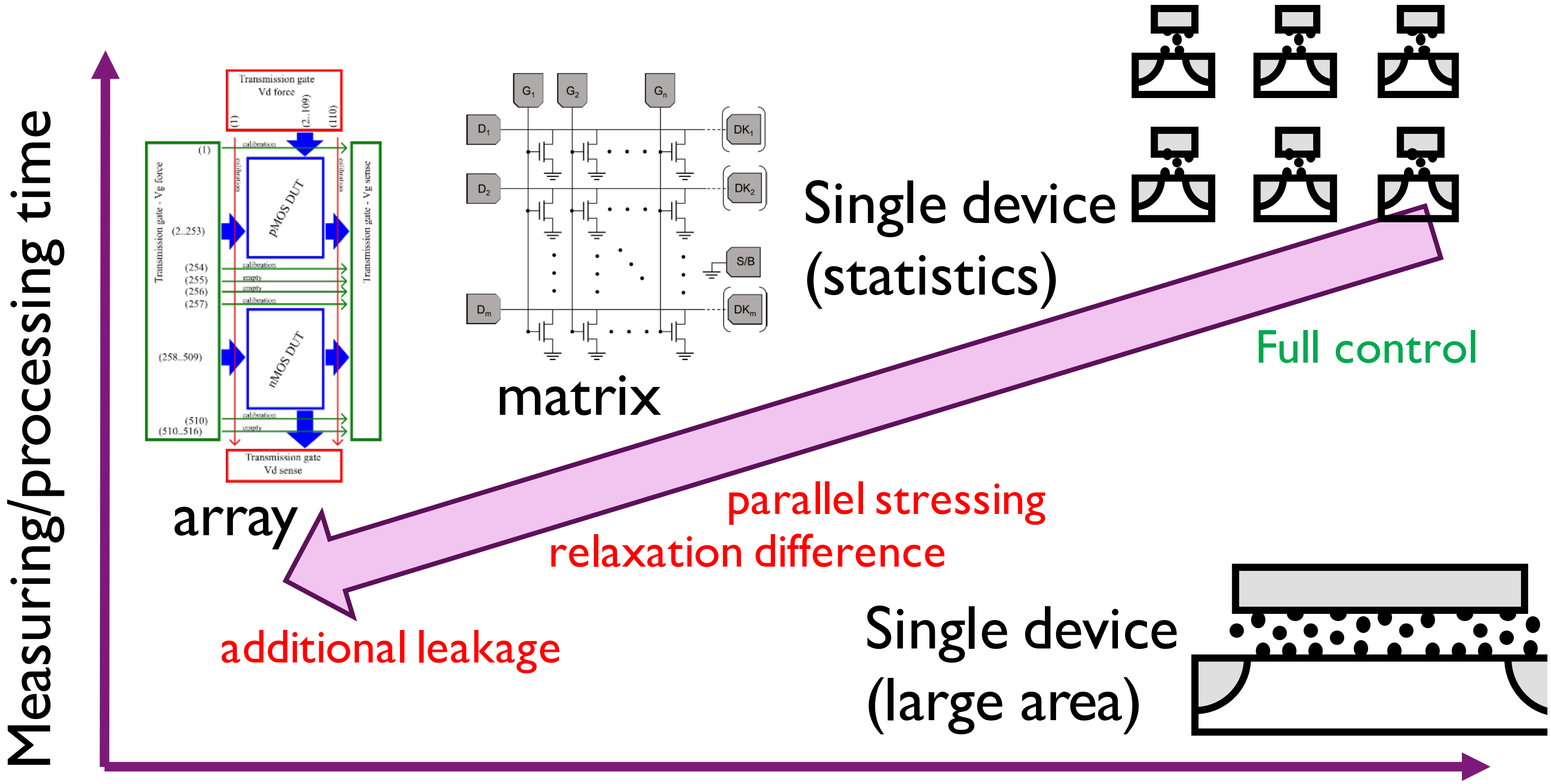




A) Large scale array for time-dependent variability analysis with bonding pads optimal for chip packaging.
B) Probing pads are added for wafer level testing.
C) Test structure for pipelined eMSM array.

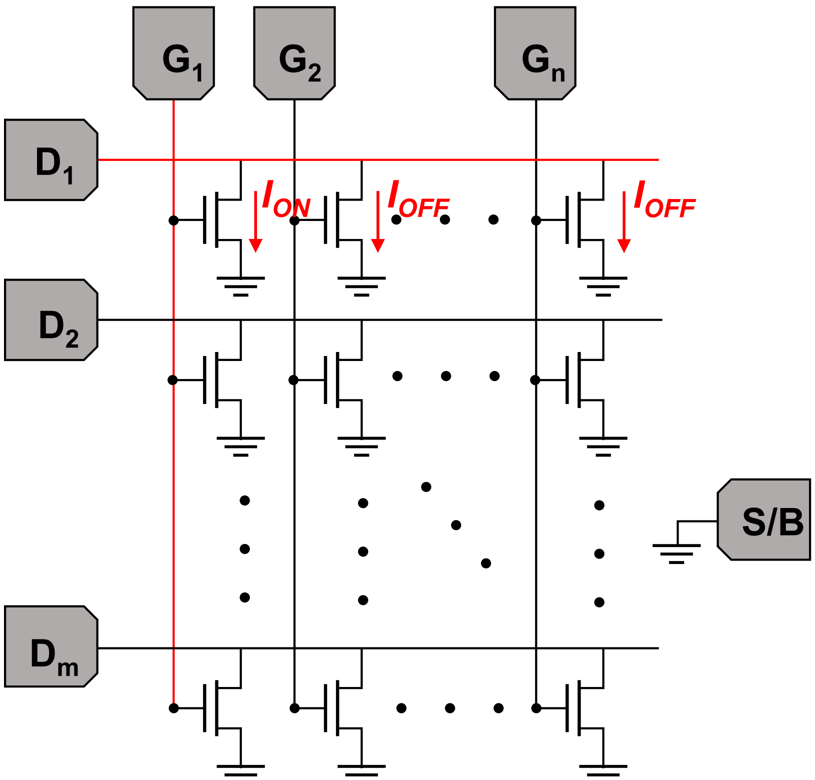
Marko Simicic *et al.*, accepted to IIRW 2015
See also V. Putcha *et al.*, IIRW 2014

LARGE SCALE ARRAYS COLLECT STATISTICAL DATA AT EXPENSE OF DUT CONTROL*



*accounted for with proper design and analysis:
pipelined measurements/optimized periphery
(Marko Simicic *et al.*, IIRW 2015, V. Putcha *et al.*, IIRW 2014)

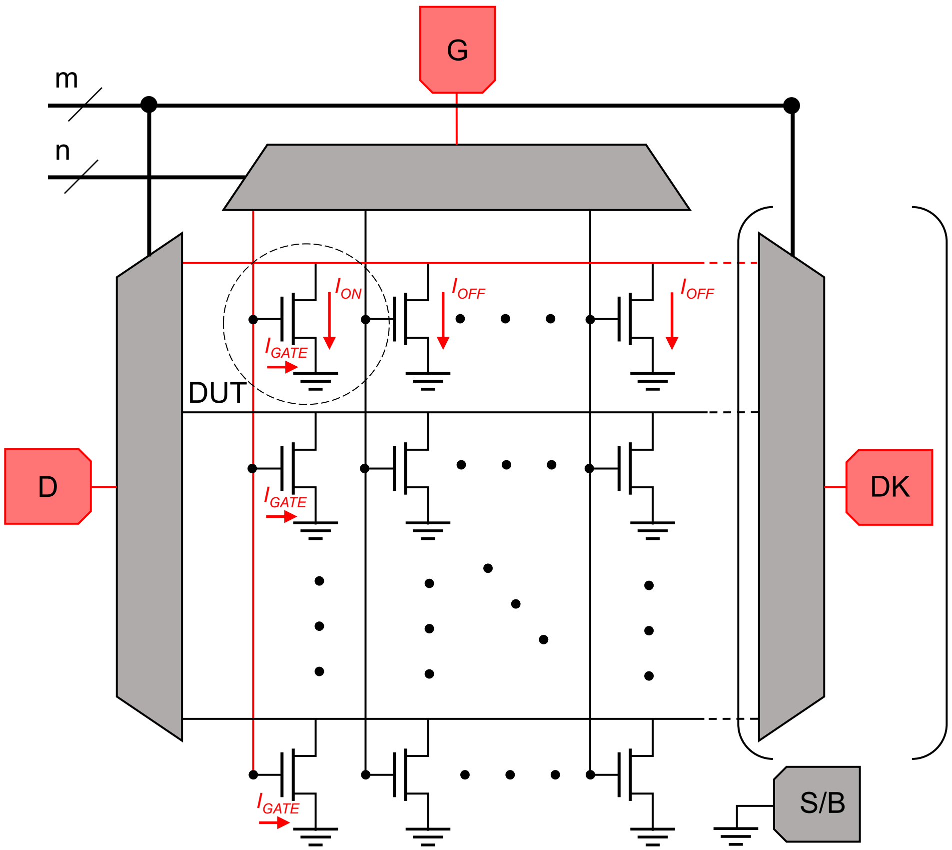
VARIABILITY MATRIX GIVES HIGH CONTROL BUT IS LIMITED BY #PADS



- Each row has common drain connection
- Each column has common gate connections
- Limited to ~100 devices

$$N_{pads} = 2m + 1(+m) = 2\sqrt{N_{devices}} + 1\left(+\sqrt{N_{devices}}\right)$$

ADDRESSABLE VARIABILITY ARRAY FOR INCREASED PAD EFFICIENCY



- Increases pad efficiency
- Gate and drain connections reduced to one pad each
- Additional pads needed for addressing

$$N_{pads} = log_2(N_{devices}) + 3(+1)$$

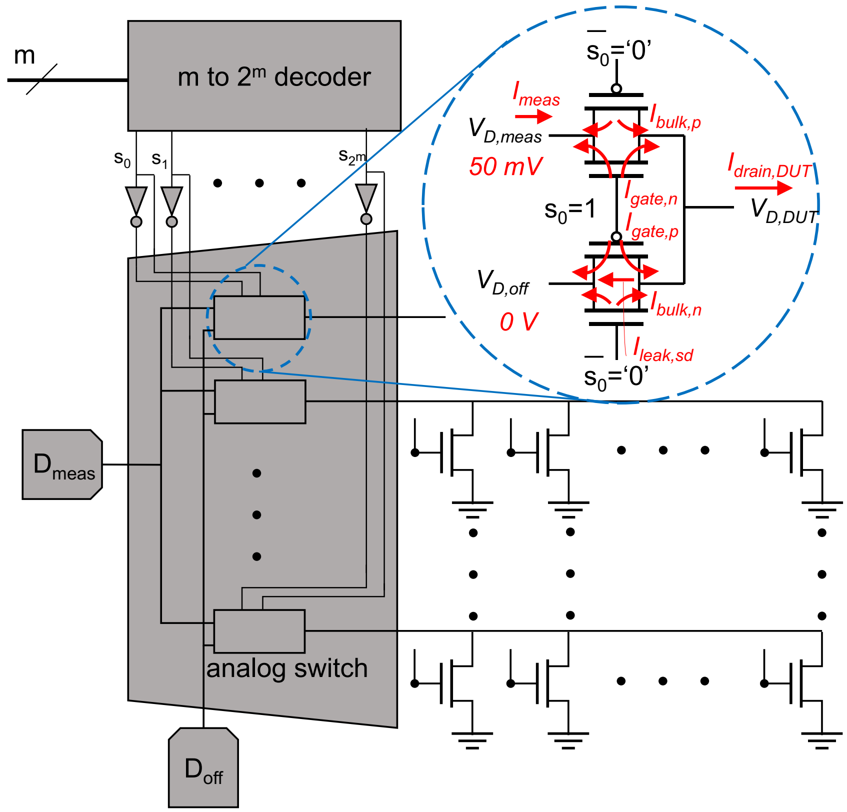
- Leakage current off-devices puts limit on number of drain columns

$$log(I_{meas}) - log(I_{off}) = \frac{V_{G,meas} - V_{G,off}}{SS}$$

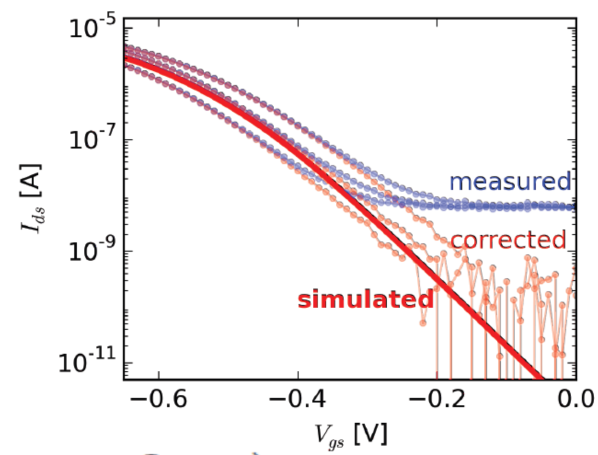
$$(n-1)I_{leak} = errI_{meas};$$

$$n = err * 10^{\left(\frac{V_{G,meas} - V_{G,off}}{SS}\right)} + 1$$

DECODER TOPOLOGIES IMPORTANT FOR ADDITIONAL LEAKAGE CONTRIBUTIONS



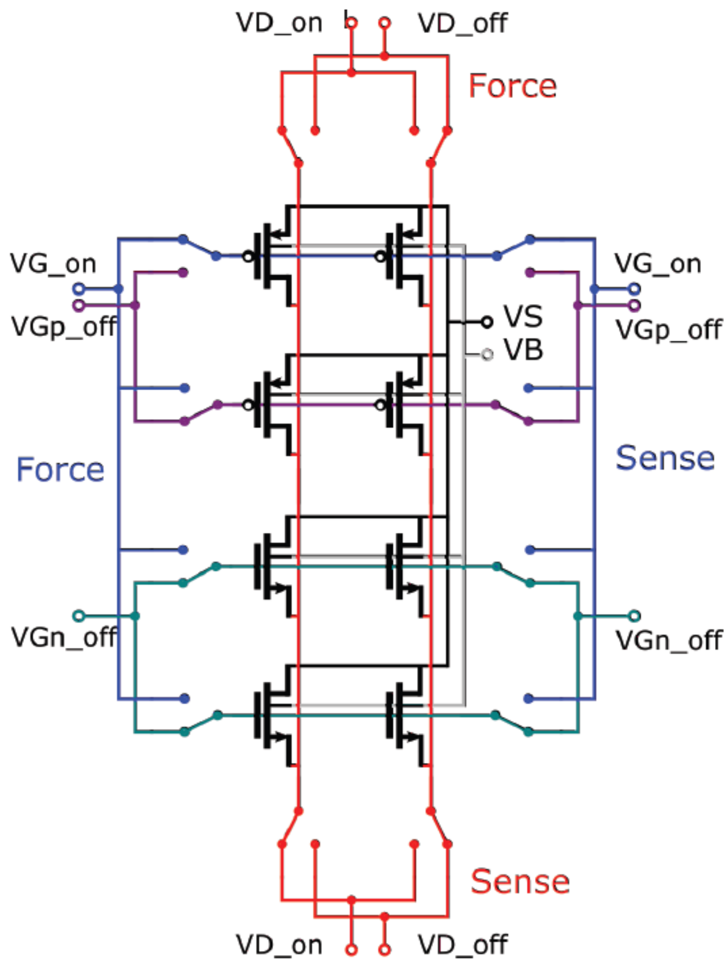
- Analog switches needed for stressing and sensing
- Typically transmission gate (p/nmos) in I/O
- Careful sizing is needed to ensure leakage is at a minimum



Marko Simicic *et al.*, IIRW 2015

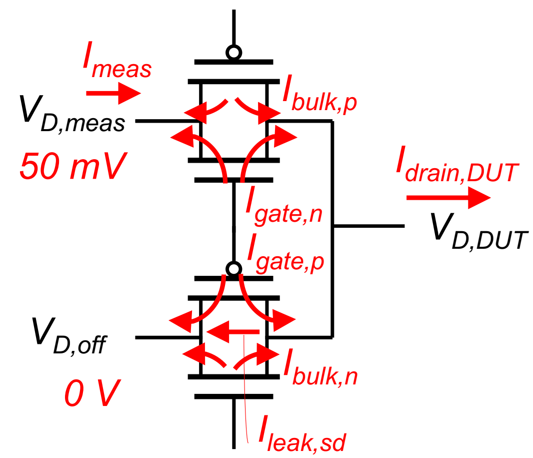
$$I_{meas} = I_{DUT} + (2^m - 1)\left(I_{leak,sd} - \frac{I_{gate,n} + I_{gate,p} + I_{bulk,n} + I_{bulk,p}}{2}\right)$$

IDEAL DUT CONTROL OBTAINED WITH KELVIN GATES AND 'OFF' VOLTAGES



- Accurately apply high bias to gate and drain
- Kelvin Gates on both drain and gate terminals
- 'Off' voltages* on both drain and gate
- Compensate for series resistance and periphery leakage currents

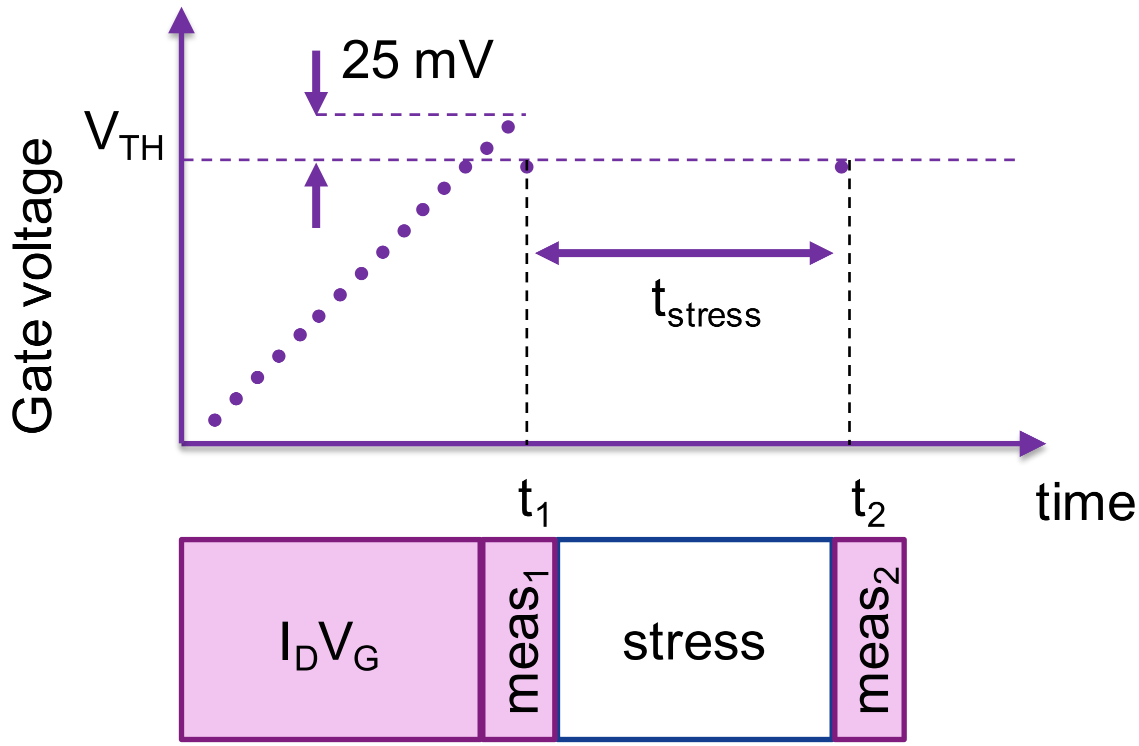
Reduce S/D leakage using $V_{D,OFF}$

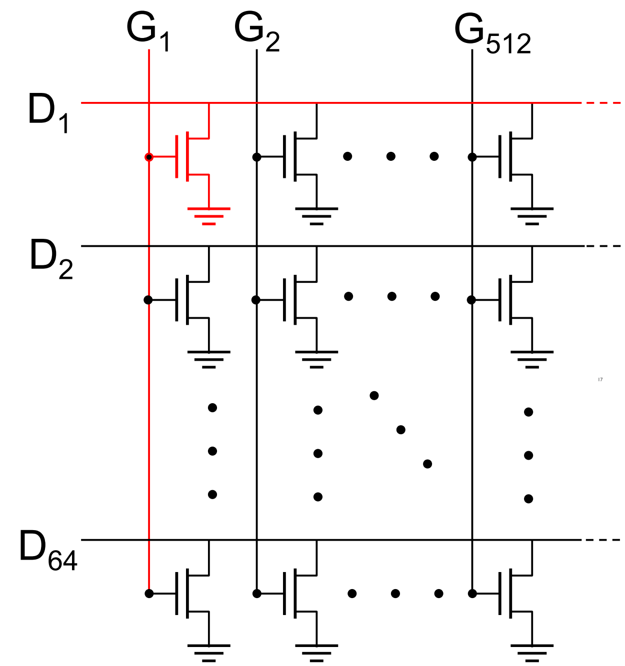


Marko Simicic *et al.*, IIRW 2015

*See also C. Chen et al., ICMTS 2014

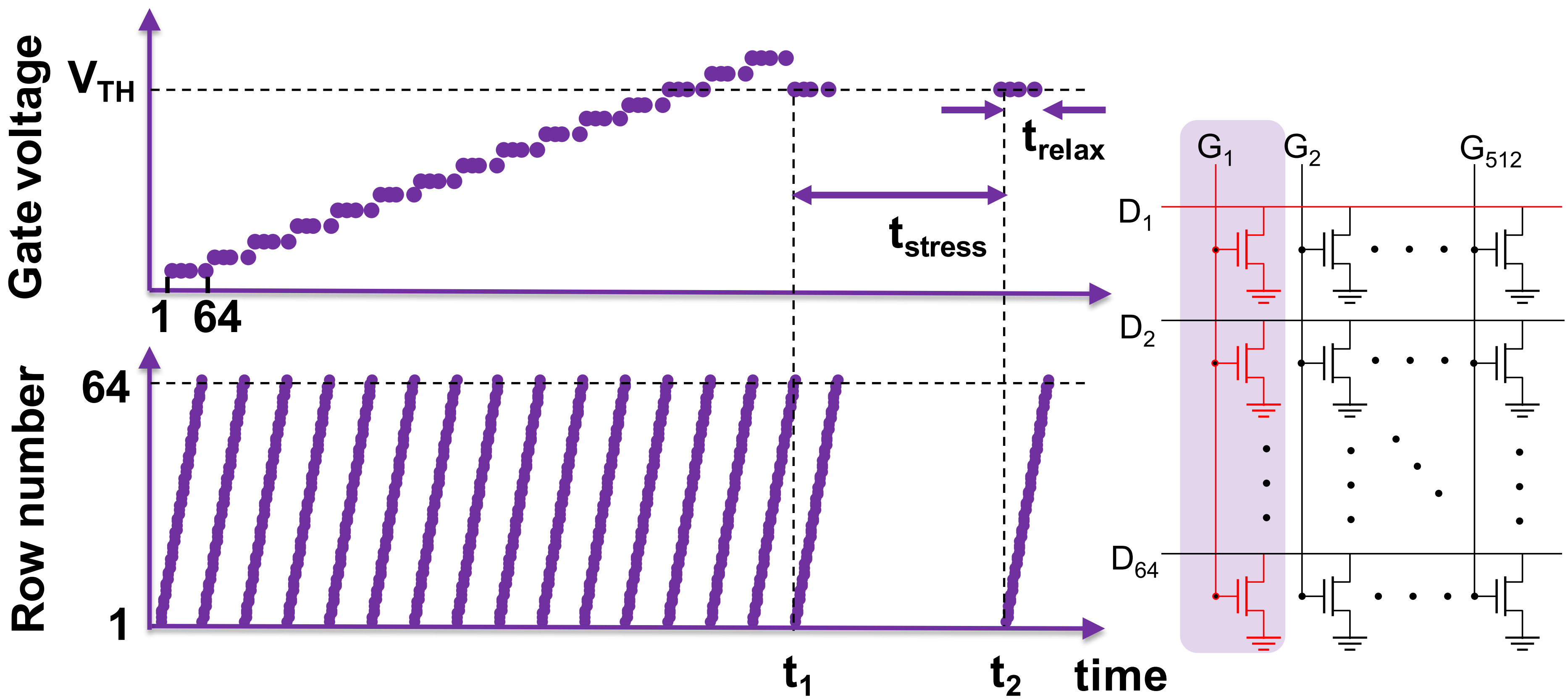
TYPICAL MEASUREMENT TO CHARACTERIZE TIME-0 AND TIME-DEPENDENT VARIABILITY





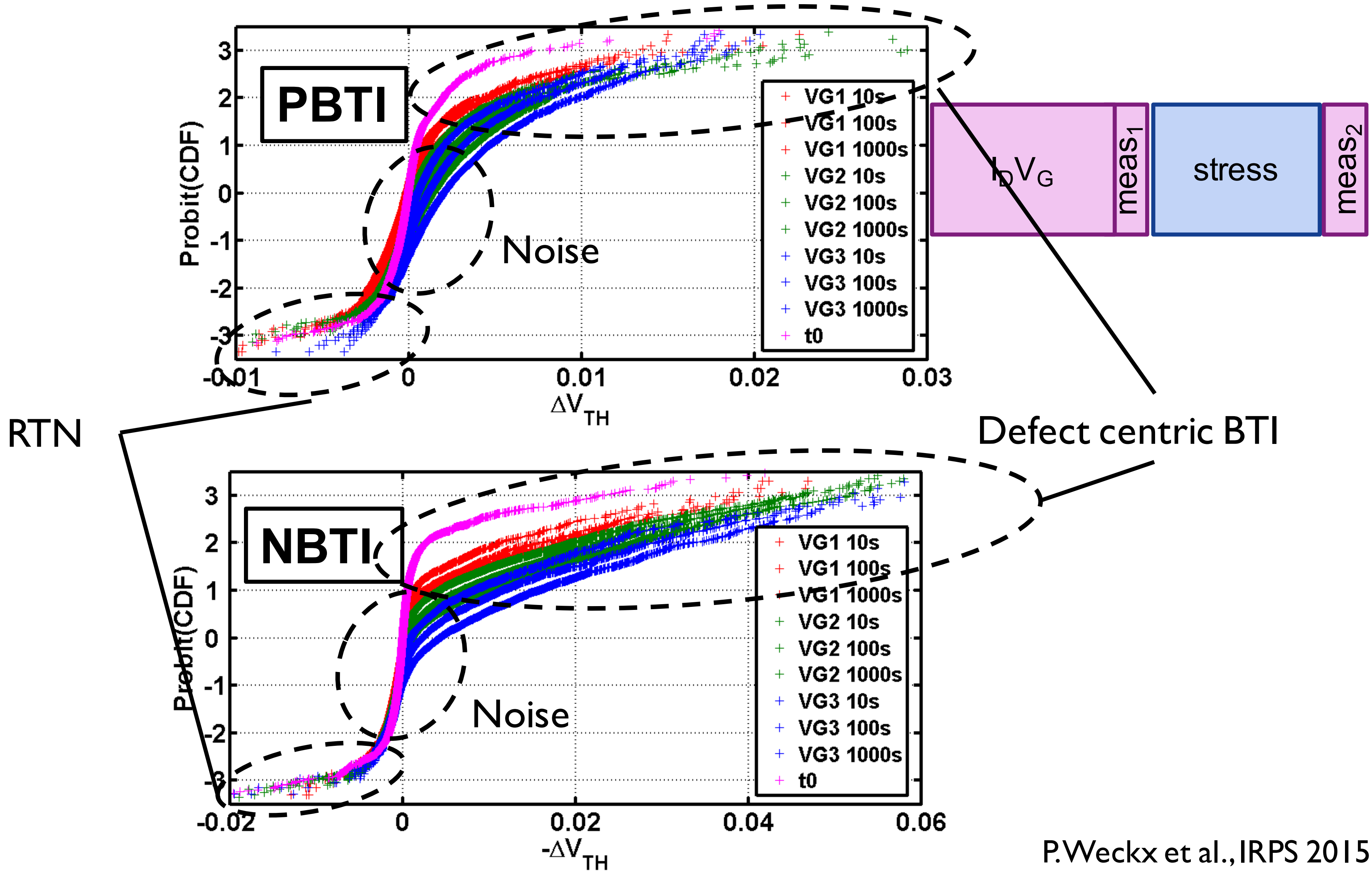
- Initial I_D-V_G with V_D=50mV and V_G swept to $|V_{TH}|$ + 50mV
- After I_D-V_G, two consecutive I_D measurements around V_G =V_{TH}
- Timing window between t_1 and t_2 can be used to apply stress on DUTs, stressing devices in parallel

MULTIPLEXING ROW MEASUREMENTS INCREASES THROUGHPUT AND REDUCES RELAXATION



- Fast serial measurements of each row DUT are necessary after the removal of stress
- For each gate voltage all rows are measured out serially
- Current traces are multiplexed

P/NBTI TIME-DEPENDENT VARIABILITY MEASURED FOR DIFFERENT VOLTAGES AND STRESS TIMES



P. Weckx et al., IRPS 2015

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- **Modeling and analyzing**
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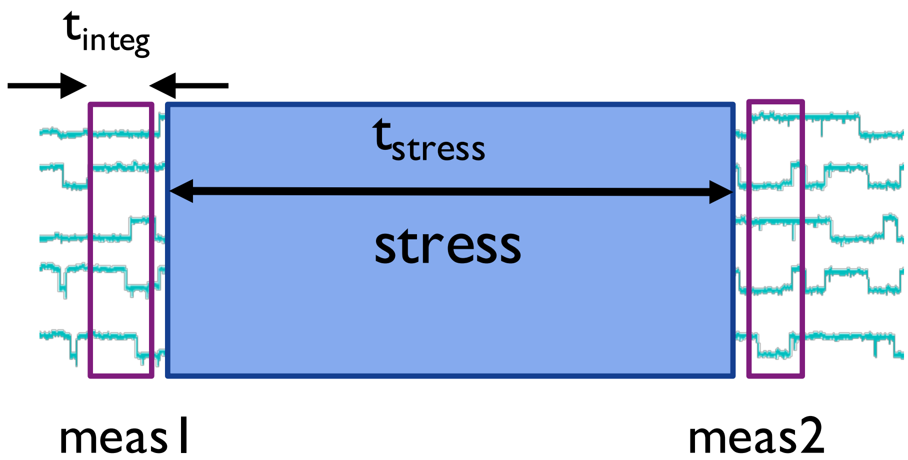
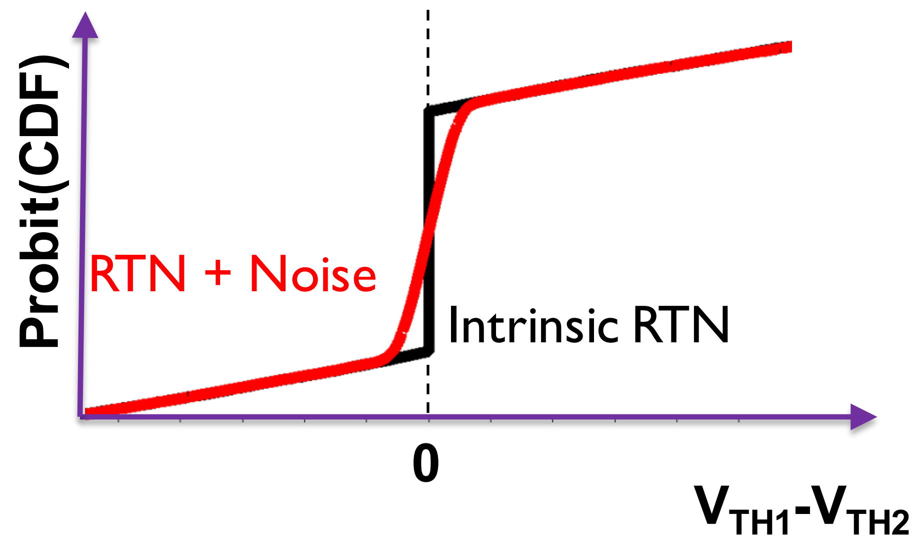
- Simulation of defect-centric model

MEASURED RTN INCORPORATES NOISE DUE TO (DIS)CHARGING DURING MEASUREMENT





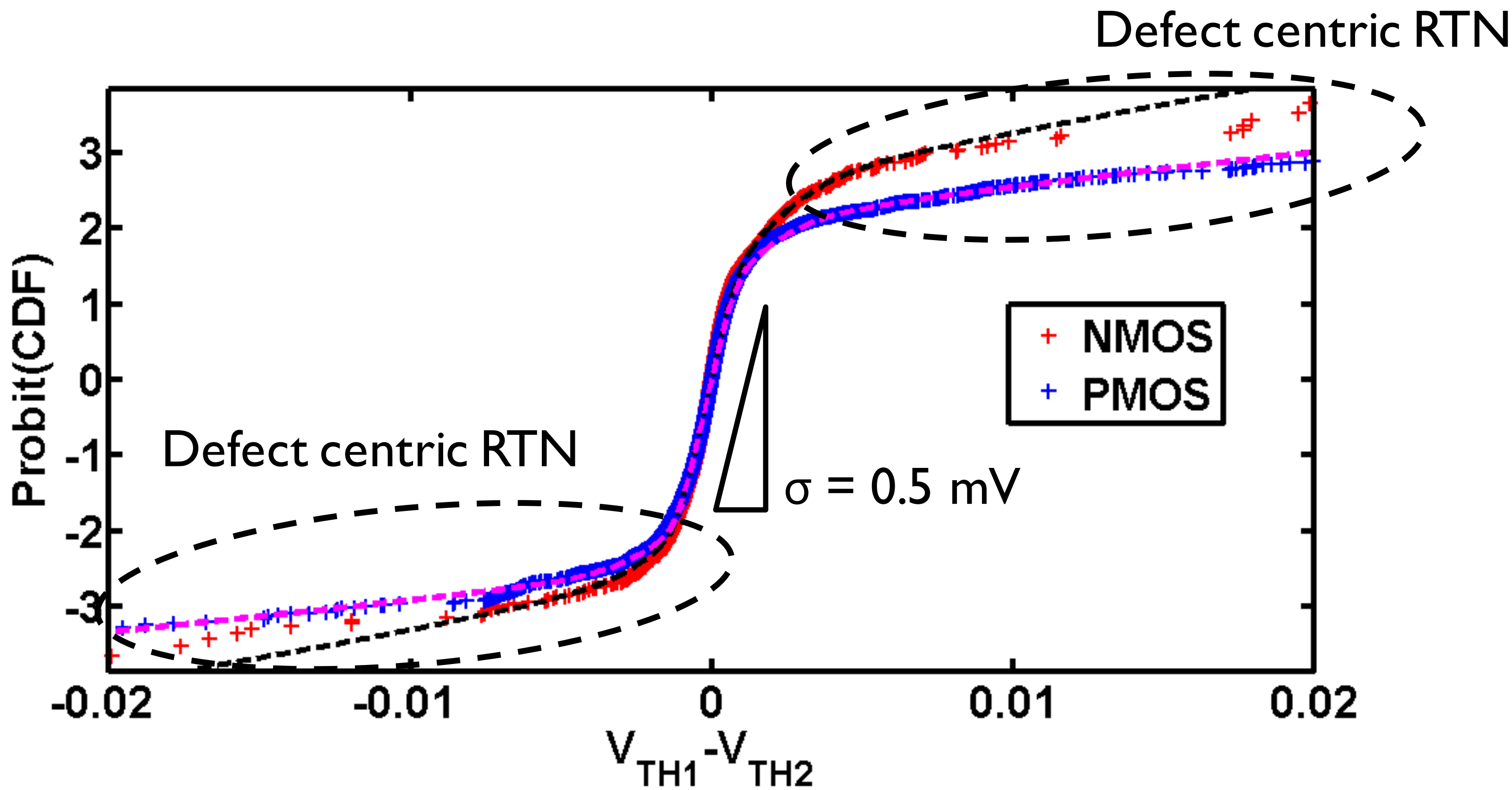
- Measured RTN incorporates noise to (dis)charging during measurement

$$\Delta V_{TH,RTN\_meas} = \Delta V_{TH,t1} - \Delta V_{TH,t2} + Noise$$

- RTN distribution for single switching traps has defect-centric tails

$$f_{RTN}(\Delta V_{TH}) = \begin{cases} f_{N,\eta}(-\Delta V_{TH}) & \Delta V_{TH} < 0 \\ 1 - 2e^{-N}\delta(\Delta V_{TH}) & \Delta V_{TH} = 0 \\ f_{N,\eta}(\Delta V_{TH}) & \Delta V_{TH} > 0 \end{cases}$$

MEASURED NOISE IS ATTRIBUTED TO RTN AND GAUSSIAN NOISE

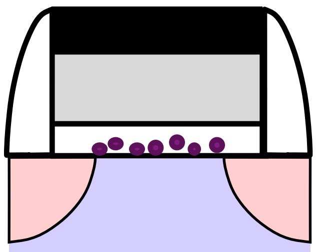


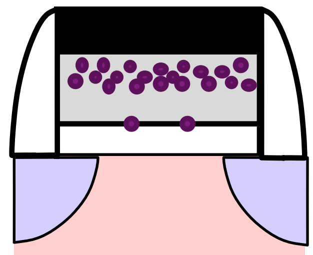
$$\Delta V_{TH,RTN\_meas} = \Delta V_{TH,t1} - \Delta V_{TH,t2} + Noise$$

$$f(\Delta V_{TH}) = f_{RTN}(\Delta V_{TH}) * f_{Gaussian}(\Delta V_{TH})$$

UNIMODAL VS BIMODAL DEFECT-CENTRIC DISTRIBUTION

e.g.
PMOS
NBTI





e.g.
NMOS
PBTI

Single defect distribution	$\Delta V_{TH} \sim Exp(\eta)$	$\Delta V_{TH,i} \sim Exp(\eta_i)$
Given #traps CDF	$F_{n,\eta}(\Delta V_{TH}) = 1 - \frac{n}{n!}\Gamma(n, \Delta V_{TH}/\eta)$	$F_{n_1,n_2,\eta_1,\eta_2}(\Delta V_{TH}) = 1 - \alpha\, exp(S\Delta V_{TH})\,1$
Distributed #traps CDF	$F_{N,\eta}(\Delta V_{TH}) = \sum_{n=0}^{\infty} \frac{e^{-N} N^n}{n!} F_{n,\eta}(\Delta V_{TH})$	$F_{N_1,N_2,\eta_1,\eta_2}(\Delta V_{TH}) = \sum_{n_1=0}^{\infty}\sum_{n_2=0}^{\infty} \frac{e^{-N_1} {N_1}^{n_1}}{n_1!} \frac{e^{-N_2} {N_2}^{n_2}}{n_2!} F_{n_1,n_2,\eta_1,\eta_2}(\Delta V_{TH})$

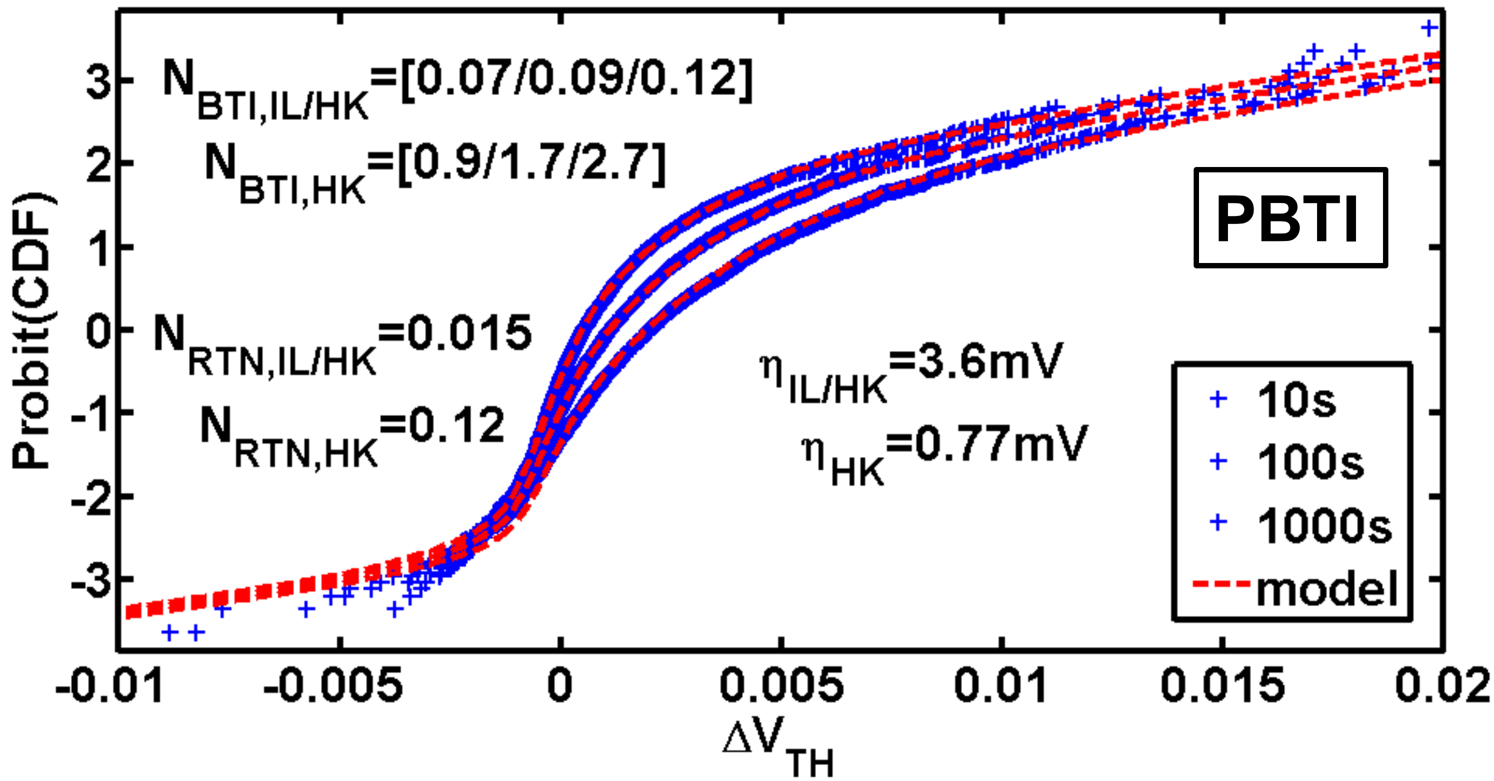
Kaczer, IRPS 2010

Weckx, IRPS 2015

Generalized CDF

$$F(\Delta V_{TH}) = \sum_{i=0}^{\infty} PDF(S_i) F_{S_i}(\Delta V_{TH})$$

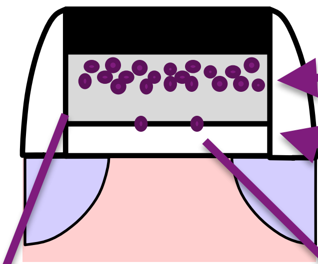
MULTIVARIATE MODEL FOR PARAMETER EXTRACTION OF RTN AND BTI



One set of η values (trapping HK and IL/HK interface) accurately models combined RTN and PBTI for various stress times

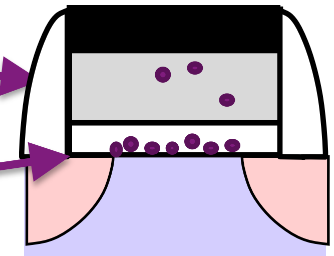
$$f(\Delta V_{TH}) = f_{BTI}(\Delta V_{TH}) * f_{RTN}(\Delta V_{TH}) * f_{Gaussian}(\Delta V_{TH})$$

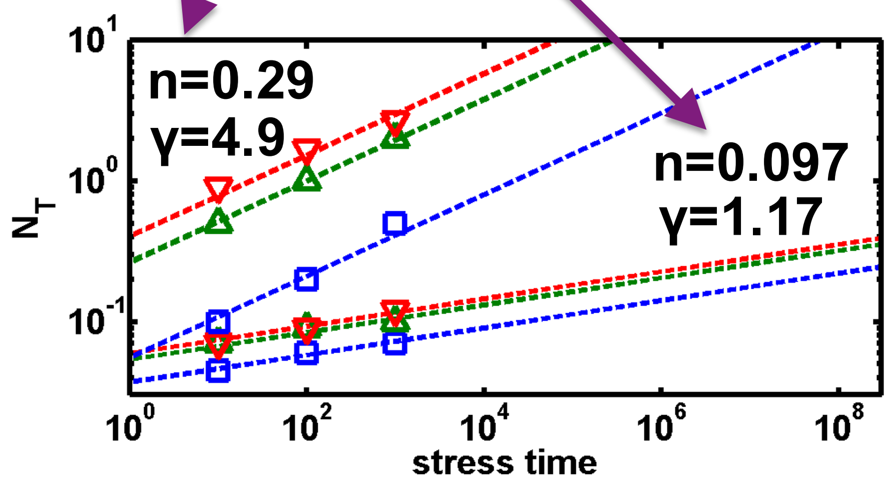
BIMODAL DEFECT CENTRIC DISTRIBUTION FOR NBTI AND PBTI, T AND V ACCELERATION

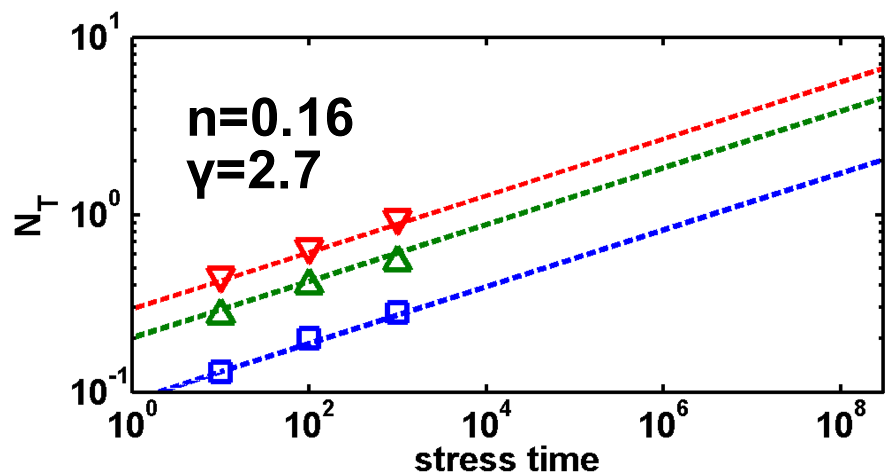


NMOS	PMOS
η=0.77mV	η=0.9mV
N_T=3.6	N_T=0.21
η=3.6mV	η=7mV
N_T=0.12	N_T=0.88

?



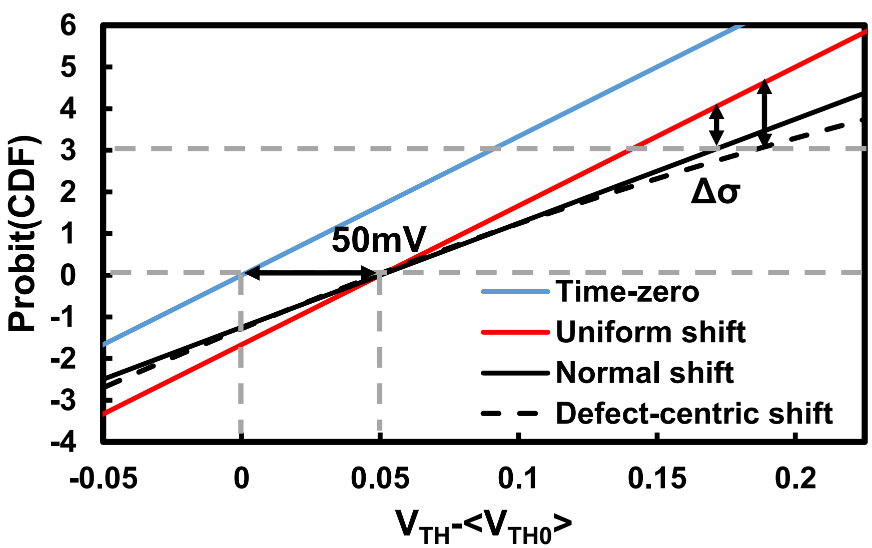


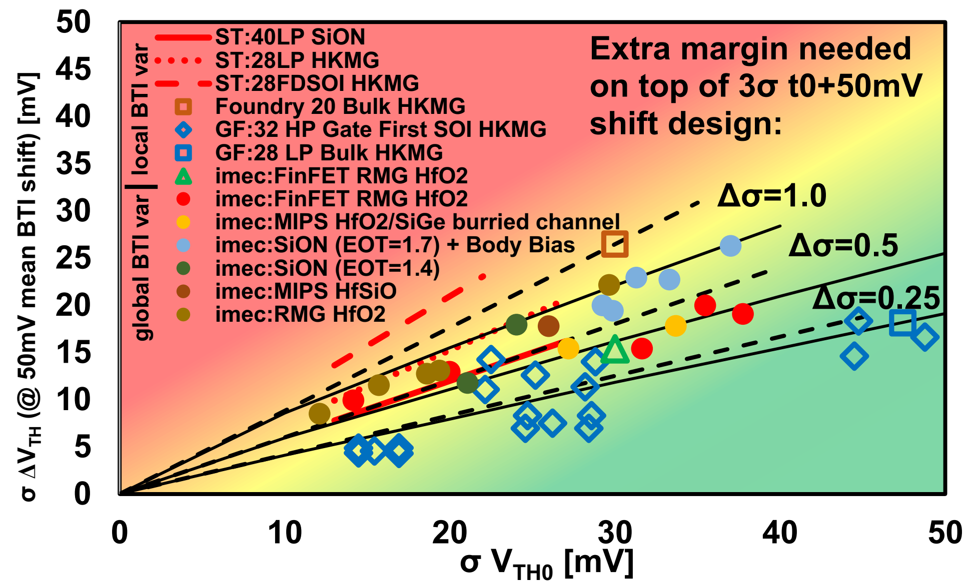


- NMOS: different components due to HK and IL/HK defects
- PMOS: high NT/high η component which is a signature for SiO_2 NBTI
- A simplified power-law model fits $N_T = AV_{OV}{}^{\gamma}t^n$

IMPORTANCE OF INCORPORATING TIME-DEPENDENT VARIABILITY DEPENDS ON THE RELATIVE IMPACT COMPARED TO TIME-ZERO VARIABILITY

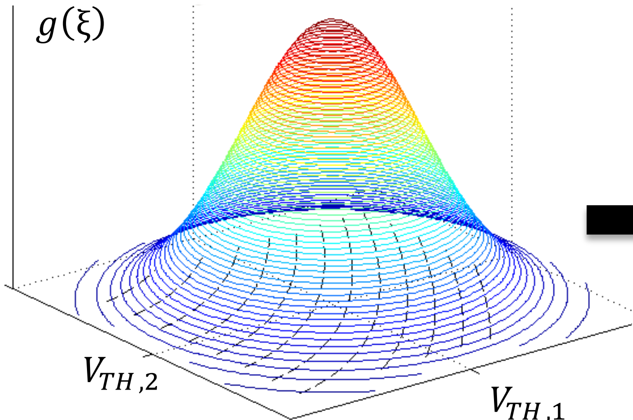
DEVICE LEVEL



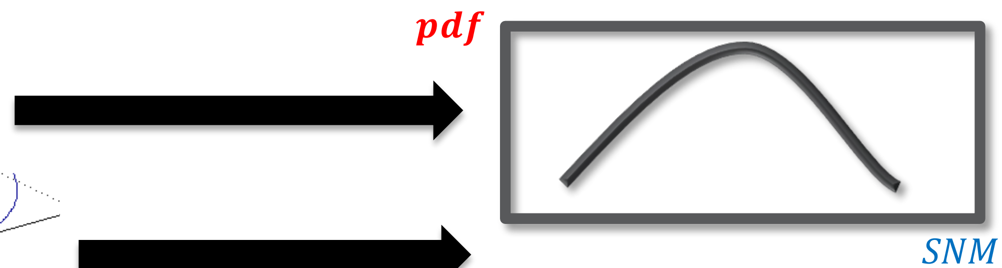


- Correlation between time-zero and time-dependent standard deviations for a 50mV mean NBTI shift
- Added sigma margin (Δσ) that needs to be adopted on top of a standard 3σ margin using either a Normal NBTI approximation (dotted) or defect-centric NBTI (solid)

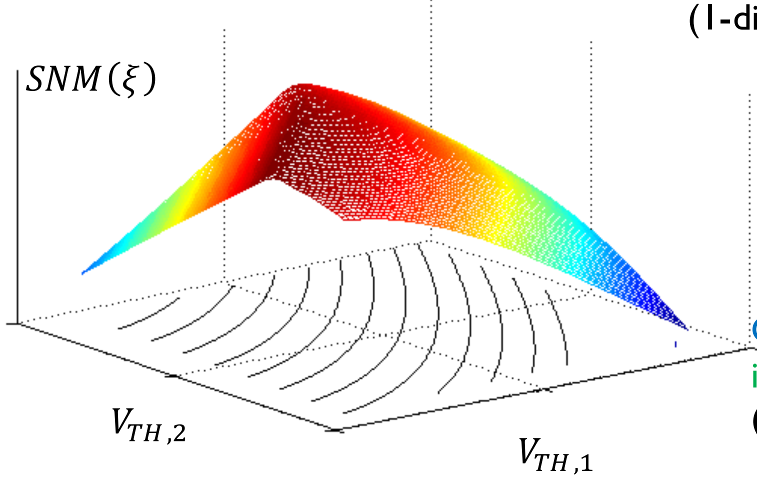
OUTPUT DISTRIBUTION OBTAINED BY PROPAGATION OF INPUT DISTRIBUTION VIA RESPONSE SURFACE



PDF as function of input parameter space (N-dimensional)



PDF as function of output (1-dimensional)

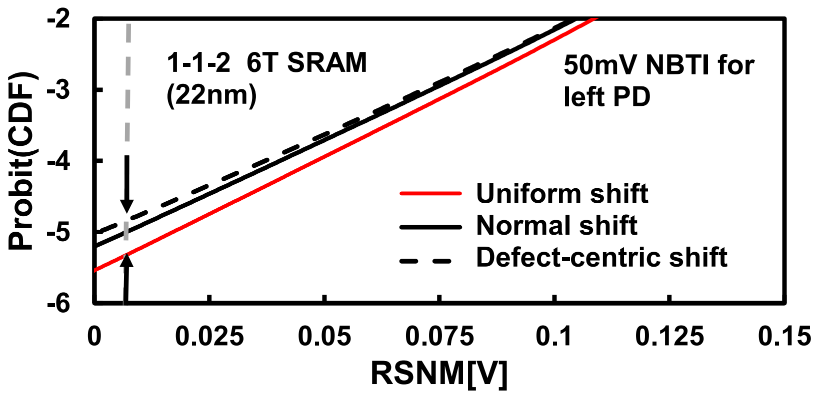


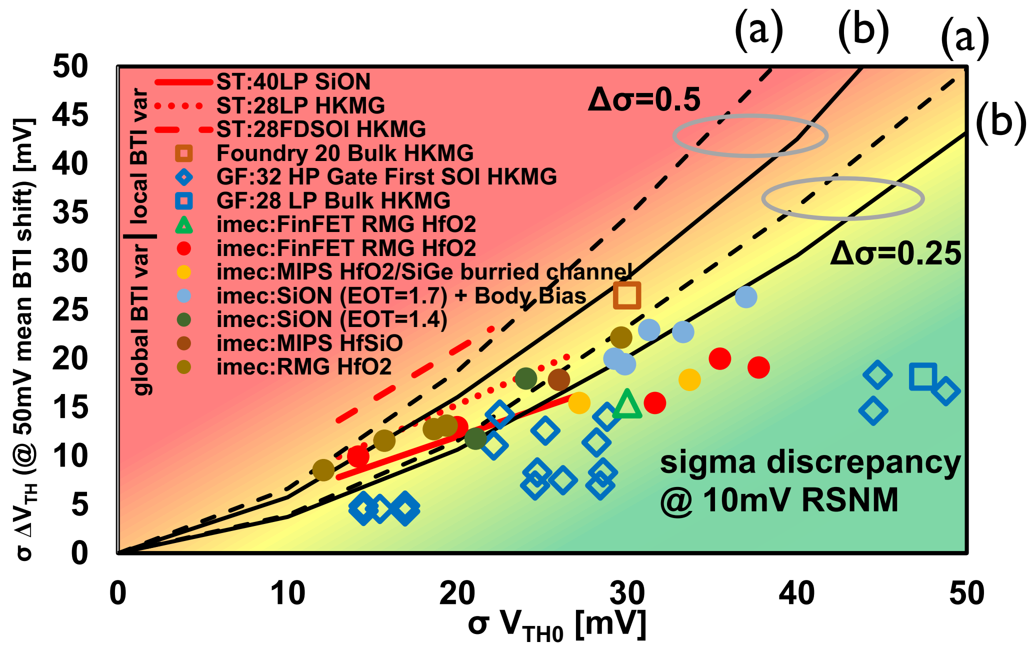
Output as function of input parameter space (N-dimensional)

P.Weckx et al., IRPS 2014

IMPORTANCE OF INCORPORATING TIME-DEPENDENT VARIABILITY DEPENDS ON THE RELATIVE IMPACT COMPARED TO TIME-ZERO VARIABILITY

SRAM CELL LEVEL





- The sigma discrepancy (Δσ) calculated for an RSNM=10mV between (a) using a uniform shift and a Normal NBTI approximation (dotted) or (b) using a uniform shift and a defect-centric NBTI (solid).

COMPLETE METHODOLOGY: FROM TEG LAYOUT, TO MEASUREMENT, ANALYSIS, PROJECTION, AND RELIABILITY-AWARE DESIGN